Doc Code: AP.PRE.REQ

PTO/SB/33 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): 05-372

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on _____

Signature _____

Typed or printed name _____

Application Number	Filed
10/534,931	May 13, 2005

First Named Inventor: Shunpu, Li

Art Unit	Examiner
1791	Brown II, David N.

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☑ attorney or agent of record. Registration number 41,962.
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

Richard A. Machonkin
Signature

Richard A. Machonkin
Typed or printed name

(312) 913-0001
Telephone number

February 9, 2010
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

(Docket No. 05-372)

In the Application of:	)	
	)	
Shunpu, Li	)	Art Unit: 1791
	)	
Serial No.: 10/534,931	)	
	)	Examiner: Brown II, David N.
Filed: May 13, 2005	)	
	)	
For: Template For Use In Manufacture Of Nanometre Scale Structures	)	Confirmation No. 3671

REASONS FOR REVIEW OF FINAL REJECTION

Applicant requests review of the final rejection mailed on October 9, 2009, because the Examiner has clearly erred in rejecting the claims.

1. The Claimed Invention

Currently pending are claims 1, 3-8, and 27, of which claim 1 is independent. Claim 1 is directed to a template formed from a layered structure. More particularly, claim 1 recites three layers: (a) "a substrate;" (b) "a single-phase polymer layer positioned on the substrate;" and (c) "a semiconductor or metal layer positioned on the polymer layer." Thus, in the layered structure of claim 1, the semiconductor or metal layer is ***on*** the polymer layer, and the polymer layer is ***on*** the substrate. Claim 1 further specifies that the polymer layer comprises a textured surface, "the texturing being caused by induction of stress in the polymer layer ***with the semiconductor or metal layer present***." Thus, the semiconductor or metal layer is positioned on the polymer layer during its texturing.

2. Status of the Claims

Independent claim 1 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Chou et al., U.S. Pub. No. 2002/0042027 ("Chou") in view of Shaper, U.S. Pub. No. 2006/0035164 ("Schaper"). Dependent claims 3-8 and 27 stand rejected in view of Chou and Shaper, and further in view of other references.

In the Response After Final filed on January 7, 2010 ("Response After Final"), Applicant submitted arguments against the rejection of claim 1 and also amended claims 4 and 8 to correct informalities. The Response After Final is incorporated herein by reference.

The Advisory Action mailed January 19, 2010 advised that Applicant's arguments in the Response After Final were fully considered but not persuasive. The Advisory Action also advised that the claim amendments in the Response After Final were entered for purposes of appeal.

3. The Examiner's Clear Error

a. The Examiner erroneously considered the "substrate" and "semiconductor layer" to be one and the same

On page 5 of the Response After Final, Applicant noted that the Examiner had erroneously regarded the silicon wafer substrate in Chou as the claimed "semiconductor layer." Chou discloses a polymer layer (PMMA) that is formed on a substrate 31 (a silicon wafer). *See* paragraph 35. But substrate 31 is not the claimed "semiconductor layer" because claim 1 recites that the "semiconductor or metal layer" is "positioned ***on*** the polymer layer." In contrast, substrate 31 in Chou is ***underneath*** the polymer layer (the PMMA layer), not positioned ***on*** the polymer layer as recited in claim 1.

In Paragraph 2 of the "Response to Arguments" section of the Advisory Action, the Examiner argued that the silicon wafer substrate in Chou corresponded to both the "substrate" and the "semiconductor layer" recited in claim 1:

> The claim requires a substrate and a semiconductor. Since the substrate is a semiconductor, both these claim requirements have been satisfied. The claim does not exclude the possibility that the two are one and the same. For this reason Chou teaches both a substrate and a semiconductor.

The Examiner is clearly wrong. The silicon wafer substrate in Chou is a semiconductor. But claim 1 also specifies where the semiconductor layer is located, in that claim 1 recites a "semiconductor ... layer ***positioned on the polymer layer***." The silicon wafer substrate in Chou is not positioned ***on*** the polymer layer (the PMMA layer). Thus, the silicon wafer substrate does not satisfy the requirements of the "semiconductor layer" of claim 1, as the Examiner has alleged.

Also clearly erroneous is the Examiner's argument that claim 1 allows the "substrate" and the "semiconductor layer" to be one and the same. In fact, claim 1 recites that the polymer layer is "positioned on the substrate" and that the semiconductor (or metal) layer is "positioned on the polymer layer." Thus, in the layered structure of claim 1, the substrate is ***underneath*** the polymer layer and the semiconductor is positioned ***on*** the polymer layer. This means that the substrate and the semiconductor layer are ***separate*** layers (i.e., separated by the polymer layer) in the layered structure of claim 1; they are not "one and the same" as the Examiner has argued.

The Examiner's confusion is also apparent in Paragraph 5 of the Advisory Action, in which the Examiner argued that the claimed "semiconductor layer" is present in Chou because it is underneath the polymer layer:

> The semiconductor layer is already present. This is the semiconductor taught by Chou. It is underneath the polymer layer.

However, claim 1 recites that the semiconductor layer is "positioned ***on*** the polymer layer," not ***underneath*** the polymer layer as disclosed in Chou.

The Examiner purported to address the claim 1 requirement of "a semiconductor or metal layer ***positioned on the polymer layer***" in Paragraph 3 of the Advisory Action. But what the Examiner cited in Chou was actually the direct opposite, namely, a polymer layer ***positioned on a semiconductor***:

> Applicant's argument that Chou does not teach a semiconductor on the polymer layer has been considered, but it is not persuasive. Chou teaches "onto the substrate 31 is a layered material ... PMMA" [0035].

The statement that "onto the substrate 31 is a layered material ... PMMA" means that the polymer layer (PMMA) is ***on*** the semiconductor (silicon wafer substrate). That clearly does not satisfy the claim 1 requirement of "a semiconductor or metal layer ***positioned on the polymer layer***."

Accordingly, the Examiner's rejection of claim 1 (and its dependent claims) is clearly erroneous and should be withdrawn.

b. Chou in view of Schaper does not teach "texturing being caused by induction of stress in the polymer layer with the semiconductor or metal layer present"

Claim 1 specifies not only that the semiconductor or metal layer is positioned on the polymer layer but also that the semiconductor or metal layer is positioned on the polymer layer during its texturing. In this regard, claim 1 recites "texturing being caused by induction of stress in the polymer layer ***with the semiconductor or metal layer present***." On pages 5-6 of the Response After Final, Applicant established that Chou does not teach a semiconductor or metal layer positioned on the polymer layer during the

texturing of the polymer layer, as recited in claim 1; in fact Chou teaches away from any modification in which an additional layer (semiconductor or metal) is positioned on the polymer layer (PMMA film 33) during its texturing. On page 7 of the Response After Final, Applicant established that Schaper does not make up for this deficiency in Chou because Schaper teaches a metal layer that is formed on the polymer layer (the PVA film) ***after*** it has been patterned.

In response, the Examiner argued: "The polymer layer of Schaper is already textured when the metal layer is added. Therefore it would not interfere with the texturing." *See* Advisory Action, Paragraph 4. But that is precisely Applicant's point. The metal layer in Schaper is added after the polymer is already textured. Thus, Schaper does not teach "texturing being caused by induction of stress in the polymer layer ***with the semiconductor or metal layer present***," as recited in claim 1. Chou also does not teach this element because the semiconductor in Chou is the silicon wafer substrate, not a "semiconductor ... layer positioned ***on*** the polymer layer," as recited in claim 1.

Accordingly, the Examiner's rejection of claim 1 (and its dependent claims) is clearly erroneous and should be withdrawn.

4. Conclusion

For the foregoing reasons, Applicant submits that the Examiner's rejections of the pending claims are clearly erroneous and that all of the pending claims should be allowed.

Respectfully submitted,

Dated: February 9, 2010

By: Richard A. Machonkin

Richard A. Machonkin
Reg. No. 41,962